Please enter the following amendments:

In the Specification:

On page 1, line 3, amend the paragraph of the Related Application section as follows:

Related Application

This application is related to ~~copending~~ patent application, U.S. Serial No. 09/542,016 entitled "Method and Apparatus for Improved Output Denormalization" filed on April 3, 2000 and assigned to the same assignee as the present application, which application is now abandoned.

On page 27, lines 5-17, amend the Abstract as follows:

Abstract of the Invention

A circuit (10) for multiplying two floating point operands (A and C) while adding or subtracting a third floating point operand (B) removes latency associated with normalization and rounding from a critical speed path for dependent calculations. An intermediate representation of a product and a third operand are selectively shifted to facilitate use of prior unnormalized dependent resultants. Logic circuitry (24, 42) implements a truth table for determining when and how much shifting should be made to intermediate values based upon ~~the~~ a resultant of a previous calculation, upon exponents of current operands and an exponent of a previous resultant operand. Normalization and rounding may be subsequently implemented, but at a time when a new cycle operation is not dependent on such operations even if data dependencies exist.